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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,404	06/12/2001	Akila Sadhasivan	42390P10595	7126

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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/880,404	SADHASIVAN ET AL.	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,19,21,25-29 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,19,21,25-29 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14, 19, 21, 25-29 and 35 are presented for examination. Claims 15-18 and 22-24 were cancelled by the amendment filed June 16, 2003. Claims 30-34 have been cancelled by the amendment filed May 19, 2005. Renumbered claim 35 was presented in the amendment filed May 19, 2005

2. A new claim was submitted with the amendment filed May 19, 2005. This claim was numbered as claim 31, however, claim 31 was cancelled by this amendment and a new claim must be the next consecutive number. Therefore this claim has been renumbered as claim 35, CFR § 1.126.

SPECIFICATION

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

NEW MATTER OBJECTION

4. The objection to claims 30-34 as containing new matter is ***withdrawn*** due to the amendment filed May 19, 2005.

CLAIM OBJECTIONS

5. The objection to claim 8 given in the final office action, dated February 26, 2005, is ***withdrawn*** due to the amendment.

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35 USC § 102

6. The rejection of claims 1-14, 19, 21 and 25-29 as being anticipated by Leak et al. is ***maintained*** from the final office action, dated February 26, 2005. This rejection includes the amended claim language.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-14, 19, 21 and 25-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Leak et al. (P/N 5,937,424)

9. Leak teaches the present invention (claim 1) as claimed including a method of performing multiple operations on a memory device with the memory device being taught as a nonvolatile memory (e.g., see the abstract), the method comprising:

dividing the memory device into k partitions, wherein k is an integer greater than or equal to two as the memory being divided or partitioned into blocks (e.g., see col. 1, line 62 to col. 2, line 59);

performing code operations from m code partitions out of k total partitions wherein m is an integer greater than or equal to one as the memory devices having code partitions (e.g., see Figures 3-5 and col. 3, lines 43-49 and col. 4, lines 1-23);

performing data operations from n data partitions out of k total partitions through low level functions accessed directly from the code partitions (e.g., see col. 3, lines 50-67) at approximately the same time as the code operations are performed from the m code partitions data operations including non-read type operations directed to operate on the partitions or blocks

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of the nonvolatile memories as the background of the reference teaching a flash EPROM can store both code and data in the flash EPROM and execute the code provided directly from the flash EPROM to the processor, as a result of the code being directly accessed from the code partition, the data would be required by the code would also need to be accessed from the data partition at approximately the same time with the example given being an erase operation (e.g., see col. 2, lines 18-29 and col. 3, lines 43-49 and col. 8, lines 1-34); and,

suspending the data operations of the n data partitions if at least one of the functions accessed directly from the code partitions determines that a preempting operation with priority is detected (e.g., see col. 8, lines 36-51) as suspending an operation which also needs data from the data partition, if the operation needing data is suspended prior to the data operation, the data operation is also suspended.

As to claim 2, Leak teaches the data partitions and the code partitions do not overlap each other in the memory device (e.g., see Figures 3-5 and col. 3, line 43 to col. 4, line 23).

As to claim 3, Leak teaches the m code partitions and the n data partitions equal the k total partitions as an inherent memory arrangement since the total number of partitions would be equal to the number of data partitions plus the number of code partitions (e.g., see col. 3, lines 43-49).

As to claim 4, Leak teaches each of the m code partitions are equal in size to each of the n data partitions as the partitions or blocks are predetermined by the use of the overall system and can be configured in a multitude of size configurations(e.g., see Figures 8A-8C and col. 3, lines 43-49 and col. 5, lines 36-45).

As to claim 5, Leak teaches the m code partitions and the n data partitions are fixed in memory space (e.g., see Figures 8A-8C and col. 5, lines 36-45).

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As to claim 6, Leak teaches the memory device is a flash memory (e.g., see Figures 8A and 8C and col. 5, lines 36-45).

As to claim 7, Leak teaches the flash memory is a flash electrically erasable read only memory (EEPROM) array (e.g., see col. 5, lines 36-45).

10. Leak teaches the present invention (claim 8) as claimed including an apparatus comprising:

logic for partitioning a memory device into a first plurality of partitions for storing code and a second plurality of partitions for storing data to enable multiple operations to be performed on the memory device at the same time as performing a program operation at the same time a suspend command is written to the command decoder (e.g., see col. 6, lines 30-48);

logic for setting each of the partitions to a status mode to track operations performed on the memory device as allowing only certain operations once a suspend command is initiated (e.g., see col. 8, line 39 to col. 9, line 4); and,

logic for determining if a first requested operation has priority over a second requested operation, wherein the logic for determining is stored within the first plurality of partitions for storing code (e.g., see col. 8, lines 39-51). Figure 1 shows the memory array control circuitry which decoding erase commands, erase suspend commands, erase resume commands, program commands, read commands and read status commands. These flash memory control circuitry is the logic for performing the commands and it is part of the flash memory device (e.g., see col. 1, lines 15-59).

As to claim 9, Leak teaches a means for saving a preempted operation before entering an interrupt routine as generating a resume command to the flash EPROM to resume program

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operation after the interrupt which means the preempted operation must be saved (e.g., see col. 8, lines 24-51).

As to claim 10, Leak teaches a means for restoring a preempted operation following an interrupt routine as generating a resume command to the flash EPROM to resume program operation after the interrupt (e.g., see Figures 7A-7B, 8A-8C and 9-10 and col. 8, lines 24-51).

11. Leak teaches the present invention (claim 11) as claimed including a memory array comprising:

a data partition (e.g., see Figures 3-5);

a code partition (e.g., see Figures 3-5);

a status mode to provide a partition status from the memory array if a task request is received by the data partition, wherein if the partition status is busy, an algorithm in the code partition determines whether the task request preempts an existing task as having status circuitry for determining the status of a partition or operation for determining whether or not to either suspend or resume operations (e.g., see Figures 6, 7A-7B, 9-10 and col. 7, line 21 to col. 9, line 33);

a read mode to enable code and data to be read from the memory array (e.g., see Figures 9-10, 11A-11B and 12); and,

a write mode to enable data to be written to the memory array (e.g., see Figures 9-10, 11A-11B and 12).

As to claim 12, Leak teaches the code is programmed into the memory array (e.g., see col. 5, line 46 to col. 6, line 14).

As to claim 13, Leak teaches the write mode enables erase operations to be performed on data stored in the memory array (e.g., see col. 6, lines 49-64).

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As to claim 14, Leak teaches the memory array is a flash memory array (e.g., see col. 5, lines 36-45 and Figures 8A and 8C).

12. Leak teaches the present invention (claim 19) as claim including an apparatus comprising:

a memory device having a code partition and a data partition, wherein the code partition includes a function that is performed on data stored in the data partition (e.g., see Figures 3-5 and col. 5, lines 34-55); and,

a flag to indicate when a suspend operation has occurred, wherein the function determines that the suspend operation has occurred if a requested second task of the data partition has priority over a first task of the data partition (e.g., see col. 6, lines 15-64 and col. 8, lines 48-51) with the function being related to an instruction stored in the code partition and thereby requiring a priority determination for execution of the function and as having status circuitry for determining the status of a partition or operation for determining whether or not to either suspend or resume operations (e.g., see Figures 6, 7A-7B, 9-10 and col. 7, line 21 to col. 9, line 33).

As to claim 21, Leak teaches the memory device is a flash memory (e.g., see col. 5, lines 36-45).

13. Leak teaches the present invention (claim 25) as claimed including a method comprising:

running a first operation of a first partition of a flash memory array with the partitions being taught as blocks (e.g., see Figure 11A-11B and col. 5, lines 36-45);

running a first operation of a second partition of a flash memory array (e.g., see Figure 11A-11B and col. 5, lines 36-45);

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requesting a second operation to be performed on the second partition with the partitions being taught as blocks (e.g., see Figure 11A-11B and col. 5, lines 36-45);

determining from the first operation of the first partition if the second operation of the second partition has a higher priority than the first operation of the second partition as certain program operations having a higher priority than an erase operation and the erase operation can therefor be preempted by the higher priority program operation (e.g., see col. 8, lines 39-51).

As to claim 26, Leak teaches suspending the first operation of the second partition if the second operation has a higher priority than the first operation as certain program operations having a higher priority than an erase operation and the erase operation can therefor be preempted by the higher priority program operation (e.g., see col. 8, lines 39-51).

As to claim 27, Leak teaches setting a flag to indicate that the first operation of the second partition must resume after the second operation is completed (e.g., see Figures 11A-11B and 12).

As to claim 28, Leak teaches running the second operation of the second partition (e.g., see Figures 11A-11B and 12).

As to claim 29, Leak teaches ignoring the request to perform the second operation of the second partition if the first operation has a high priority than the second operation as certain program operations having a higher priority than an erase operation and the erase operation can therefor be preempted by the higher priority program operation (e.g., see col. 8, lines 39-51).

As to claim 35, Leak teaches the functions accessed directly from the code partitions comprises the functions accessed from the code partitions without first copying the functions to another memory device (e.g., see col. 3, lines 50-67).

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35 USC § 102(e)

14. The rejection of claims 19 and 21 as being anticipated by Brown et al. is ***maintained*** and repeated below. This rejection is withdrawn for claim 20. This rejection includes the amended claim language.

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

16. Claims 19 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated Brown et al. (P/N 6,201,739 B1)

17. Brown teaches the invention (claim 19) as claimed including an apparatus comprising:

a memory device having a code partition and a data partition, wherein the code partition comprises a low level function that is performed on data stored in the data partition as the functionality of suspending erase operations on any block in the memory device including the blocks comprising the data partition (e.g., see col. 5, lines 46-67); and,

a flag to indicate when a suspend operation has occurred (e.g., see Figures 10-14 and col. 12, lines 39-65) wherein the function determines that the suspend operation has occurred if a requested second task of the data partition has a priority than a first task of the data partition as having status circuitry for determining the status of a partition or operation for determining whether or not to either suspend or resume operations (e.g., see Figures 6, 7A-7B, 9-10 and col. 7, line 21 to col. 9, line 33 and col. 12, line 39 to col. 13, line 56).

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As to claim 21, Brown teaches the memory device is a flash memory (e.g., see col. 5, lines 22-35).

35 USC § 103

18. The rejection of claims 1-14 and 25-29 as being unpatentable over by Hazen et al. in view of Brown et al. is ***maintained*** repeated below. This rejection includes the amended claim language.

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1-14 and 25-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Hazen et al. (P/N 6,088,264) in view of Brown et al. (P/N 6,201,739 B1).

21. Hazen teaches the invention (claims 1 and 8) as claimed including a method of performing multiple operations on a memory device, the method comprising:

dividing the memory device into k partitions, wherein k is an integer greater than or equal to two as partitioning a flash memory into partitions (e.g., see Figures 2-3 and col. 3, lines 29-59);

performing code operations from m code partitions out of k total partitions, wherein m is an integer greater than or equal to one as the memory device being partitioned such that a first partition is used to store data while a different second partition stores code and a third partition is used for updating the code (e.g., see col. 3, lines 44-59); and,

performing data operations from n data partitions out of k total partitions through low level functions accessed directly from the code partitions (e.g., see col. 1, lines 44-49) at

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approximately the same time as the code operations are performed form the m code partitions wherein n is an integer greater than or equal to one as having the ability to either update the code utilizing a third partition while the original code in the second partition is concurrently executing as well the condition of executing code from a first partition while updating data in a second partition (e.g., see col. 3, lines 44-59).

Hazen does not specifically teach the method step of suspending the data operations of the n data partitions if a preempting operation is detected, however, Brown teaches using a preempt pin to suspend operations in a flash memory device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the preempt pin arrangement with the partitioned flash memory device as taught by Hazen because the suspension of a command allows greater flexibility and longevity for flash memory devices by utilizing a more sophisticated control structure rather than always erasing and writing to a flash memory device which has a limited number of times for being written to and erased. By incorporating a preempt or suspend operation with the flash memory code fetching data from the data partition operations is also preempted or suspended under certain conditions because the code must use data from the data partition for the operation. The command decoder and command latches decode read and read status to the data partition and therefore allow these commands to be preempted or suspended similarly to the preemption or suspension of the execution of code held in the code partition.

Hazen does not specifically teach determining from the first operation of the first partition if the second operation of the second partition has a higher priority than the first operation of the second partition, however, Brown teaches being able to suspend operations depends upon which operations being executed which inherently requires determining the

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priority of execution of the code (e.g., see Figures 11-14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brown with the teachings of Hazen because this functionally allows the completion of the operation without requiring extensive resetting or restarting of the program or activity and thereby allows for a more concise and accurate operation of the device.

As to claim 2, Hazen teaches the data partition and the code partitions do not overlap each other in the memory device (e.g., see Figures 2-3 and col. 3, lines 16-23).

As to claim 3, Hazen teaches the m code partitions and the n data partitions equal the k total partitions as there being three total partitions with one data partition and two code partitions (e.g., see Figures 2-3 and col. 3, lines 38-59).

As to claim 4, Hazen teaches each of the m code partitions are equal in size to each of the n data partitions as one of the possibilities for the multi-partitioned flash memory device, i.e. the partitions can be either the same size or different sizes (e.g., see col. 2, lines 23-43).

As to claim 5, Hazen teaches the m code partitions and the n data partitions are fixed in memory space (e.g., see col. 2, lines 23-43).

As to claim 6, Hazen teaches the memory device is a flash memory (e.g., see col. 2, lines 23-43).

As to claim 7, Hazen teaches the flash memory is a flash electrically erasable read only memory (EEPROM) array (e.g., see col. 1, lines 9-18).

As to claims 9 and 10, Hazen does not specifically teach a means for saving a preempted operation before entering an interrupt routine and then restoring a preempted operation following an interrupt routine, however, Brown teaches both erase suspend circuitry and program suspend circuitry with latches to maintain the operations in order to resume either the erase function or

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the program function which was suspended (e.g., see Figure 9 and col. 7, line 19 to col. 8, line 25)). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brown with the teachings of Hazen because this functionally allows the completion of the operation without requiring extensive resetting or restarting of the program or activity and thereby allows for a more concise and accurate operation of the device.

22. Hazen teaches the invention (claim 11) as claimed including a memory array comprising:

a data partition (e.g., see Figures 2-3 and col. 3, lines 38-59);

a code partition (e.g., see Figures 2-3 and col. 3, lines 38-59);

a status mode to provide a partition status from the memory array if a task request is received by the data partition (e.g., see col. 2, lines 60-64 of Hazen), wherein if the partition status is busy, an algorithm in the code partition determines whether the task request preempts an existing task is better taught by the secondary reference, Brown et al. Brown also uses status registers for each partition (e.g., see col. 6, line 47 to col. 7, line 18) and it is inherent that an algorithm exist for a task being preempted as this is a normal program activity for when a conflict for using the same memory location is executed, for instance, in order to maintain data coherency there are times writes must take place before a read to a memory location for vice versa – this is typical of any memory device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brown with the teachings of Hazen as Brown is providing details and more complete circuitry for a function which Hazen must also implement as every memory device must maintain coherency with the other memory within the system as well as with the execution sequence of the algorithms or code being executed; and,

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a read mode to enable code and data to be read from the memory array (e.g., see col. 2, lines 16-22); and;

a write mode to enable data to be written to the memory array (e.g., see col. 2, lines 16-22).

As to claim 12, Hazen teaches the code is programmed into the memory array (e.g., see col. 3, lines 38-59).

As to claim 13, Hazen teaches the write mode enables erase operations to be performed on data stored in the memory array (e.g., see col. 2, line 65 to col. 3, line 19).

As to claim 14, Hazen teaches the memory array is a flash memory array (e.g., see (e.g., see col. 1, lines 9-18).

23. Hazen teaches the invention (claim 25) as claimed including a method comprising:

running a first operation of a first partition of a memory array as executing an operation (e.g., see col. 3, lines 38-59);

running a first operation of a second partition of the memory array as the ability to access each partition independently (e.g., see col. 3, lines 38-59); and,

Hazen does not specifically teach determining from the first operation of the first partition if the second operation of the second partition has a higher priority than the first operation of the second partition, however, Brown teaches being able to suspend operations depends upon which operations being executed which inherently requires determining the priority of execution of the code (e.g., see Figures 11-14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brown with the teachings of Hazen because this functionally allows the completion of the operation

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without requiring extensive resetting or restarting of the program or activity and thereby allows for a more concise and accurate operation of the device.

As to claim 26, Brown teaches suspending the first operation of the second partition if the second operation has a higher priority than the first operation as Brown being suspend operations depend upon which operations being executed which requires determining the priority of execution of the code (e.g., see Figures 11-14).

As to claim 27, Brown teaches setting a flag to indicate that the first operation of the second partition must resume after the second operation is completed (e.g., see Figures 11-14).

As to claim 28, Brown inherently teaches running the second operation of the second partition.

As to claim 29, Brown teaches ignoring the request to perform the second operation of the second partition if the first operation has a higher priority than the second operation as the ability to suspend operations as necessary (e.g., see Figures 11-14).

As to claim 31, Hazen teaches the functions accessed directly from the code partitions comprises the functions accessed from the code partitions without first copying the functions to another memory device (e.g., see col. 1, lines 44-49).

Response to Applicant's Remarks

24. Applicant's arguments filed May 19, 2005 have been fully considered but they are not persuasive for all the rejections.

25. As to Leak not teaching or disclosing functions accessed directly from the code partition to be used to perform data operations, this limitation is taught in the background of the invention of the reference.

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26. As to Leak teaching away from a suspend function being stored within a code partition of a memory device, the erase suspend logic is part of the flash memory device. Figure 6 shows a block diagram of the parts of the memory device, this is not a teaching of separate chips for the command register, element 120, the memory array control circuitry, element 140 and the memory array.

27. As to Brown not teaching or disclosing storing a function within flash EPROM for determining when a suspend operation has occurred if a requested second task has priority over a first task is taught as operations having different priorities (e.g., see col. 12, line 39 to col. 13, line 56).

28. As to Brown not teaching or disclosing the flash EPROM includes the function that determines the suspend operation has occurred including there being a bit in the status word that indicates an operation is suspended, an erase operation is suspended or a program operation is suspended (e.g., see col. 12, lines 52-65).

29. As to Brown teaching away from the invention by indicating that system suspend circuitry contains the suspend logic, not flash EPROM as the option of having the suspend circuitry be part of the system but the reference also teaches the suspend/resume circuitry is part of the command register of the EPROM or the memory array control circuitry (e.g., see col. 8, lines 26-34).

30. As to the combination of Hazen and Brown not teaching or disclosing suspending data operations if a function accessed directly from a code partition determines that a preempting operation with priority is detected, this limitation is taught to the extent required by the actual claim language. Brown teaches preempting an operation which includes suspending a data operation when a higher priority operation is to be processed (e.g., see col. 12, lines 39-65).

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31. As to Brown not teaching or disclosing a suspend or preempting function residing within flash EPROM itself, the reference states this circuitry can be part of the system or part of the EPROM.

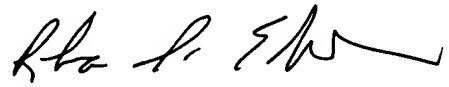
32. As to Brown teaching or suggesting away from the invention by indicating that external system suspend circuitry contains the suspend logic, not flash EPROM, the suspend/resume circuitry resides in the command register or within the memory array control circuitry which are both part of the EPROM (e.g., see col. 8, lines 26-34).

CONCLUSION

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.



Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

August 19, 2005

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